Reg. No: ☐☐☐☐☐☐☐☐☐☐

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY:: PUTTUR
(AUTONOMOUS)
B. Tech II Year I Semester Supplementary Examinations December-2021
ELECTRONIC DEVICES
(Electronics and Communication Engineering)

Time: 3 hours   Max. Marks: 60

PART-A
(Answer all the Questions 5 x 2 = 10 Marks)

1	a	Define barrier potential.	L1	2M
	b	Compare half wave rectifier and Full wave rectifier.	L2	2M
	c	What do you mean by Punch through Effect?	L1	2M
	d	Draw the generalized hybrid model for BJT amplifier.	L2	2M
	e	Define Pinch off Voltage	L1	2M

PART-B
(Answer all Five Units 5 x 10 = 50 Marks)

UNIT-I

2	a	What is a PN Junction? Explain the formation of depletion layer in a PN junction.	L2	5M
	b	Derive the Diode Current Equation.	L1	5M

OR

3	a	Mention the importance of Diffusion capacitance.	L1	2M
	b	Derive the expression for Diffusion capacitance of a PN Junction Diode.	L3	8M

UNIT-II

4	a	Draw the circuit diagram of Full wave rectifier and explain its operation with the help of waveforms.	L2	5M
	b	Derive the expressions for Ripple Factor and Efficiency of Full Wave Rectifier.	L1	5M

OR

5	a	Draw and discuss the VI characteristics of a Zener Diode.	L2	5M
	b	Derive the expression for ripple factor of inductor filter.	L3	5M

UNIT-III

6	a	Discuss the operation of NPN transistor with diagram.	L2	5M
	b	If the base current in a transistor is 20µA when the emitter current is 6.4mA, what are the values of α and β? Also calculate the collector current.	L3	5M

OR

7		Derive the condition for Thermal Stability to avoid thermal runaway.	L3	10M

UNIT-IV

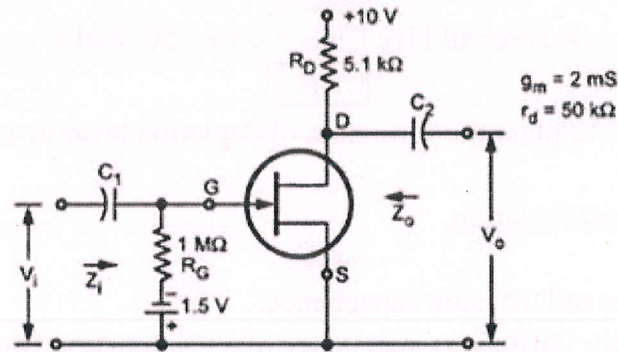|				
8	a	Determine the parameters AI, Ri, Av and R0 of Emitter Follower using simplified hybrid model analysis.	L3	5M
	b	voltage source of internal resistance Rs = 900Ω drives a CC amplifier using load resistance RL=2000Ω. The CE h parameters are hfe=60, hie=1200Ω, hoe = 25µA/V and hre = 2 x 10-4. Compute AI, Ri, Av and R0 using approximate analysis.	L3	5M

OR

9 a Draw the circuit diagram of a single stage RC coupled Amplifier and discuss the   **L2**   **5M**
       steps used for designing it.

   b Determine Voltage Gain, Current Gain, Input resistance and Output resistance for   **L3**   **5M**
       a CE amplifier using NPN transistor with $h_{ie} = 1200\Omega$, $h_{re} = 0$, $h_{fe} = 36$ and $h_{oe} = 2 \times 10^{-6}$ mhos, $R_L = 2.5k\Omega$ and $R_S = 500\Omega$ (neglect the effect of biasing circuit).

UNIT-V

10 a Describe the construction and working principle of N-channel JFET.   **L2**   **5M**

    b Mention the applications of JFET.   **L1**   **5M**

OR

11 a Draw and explain the small signal model of FET at low frequency.   **L1**   **4M**

    b For the circuit shown in Fig. determine input impedance, output impedance and   **L4**   **6M**
       voltage gain.

END